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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/729,721	12/05/2003	Salvatore Leonardi	856063.672D1	2634

38106 7590 03/25/2005

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EXAMINER	
IM, JUNGHWA M	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 03/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/729,721	LEONARDI ET AL.	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-7,9-15,27 and 28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-7,9-15,27 and 28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/05/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election of claims 1-3, 5-7, 9-15 and 27-28 in the reply filed on February 23, 2005 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 5, 7, 14 and 28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 5 recites an unclear limitation of "fill polysilicon that has been enhanced by implantation."

Claim 7 recites an unclear limitation of "said first polysilicon layer is enhanced by angled implantation and has a thickness dimension conforming to the sidewalls of the dielectric region to prevent said region from becoming filled completely." The figures of the instant invention show that the trenches are filled completely.

Claim 14 and 28 recite an unclear limitation of "the first layer of polysilicon is implanted by angled implantation and has a thickness dimension conforming to the walls of the

dielectric-coated at least one trench to prevent complete filling of the at least one trench." The figures of the instant invention show that the trenches are filled completely.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 9-10 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Ando (JP 08-032030).

Regarding claim 9, Fig. 1 of Ando shows an integrated resistive structure, comprising:

at least one trench formed in a semiconductor substrate [1] to have a depth greater than a depletion region;

a dielectric layer [3] formed of a dielectric oxide [silicon oxide; Example paragraph 0019] entirely coating all walls of the at least one trench; and

a polysilicon region [4; a doped polysilicon] filling the at least one trench to be isolated dielectrically from the semiconductor substrate, the polysilicon region having at least a portion that is doped.

Regarding claim 10, Fig. 1 of Ando shows the dielectric layer has vertical and horizontal dimensions that are greater than vertical and horizontal dimensions of the polysilicon region (abstract).

Regarding claim 12, Fig. 1 of Ando shows the polysilicon region includes a doped surface region through forming doped polysilicon.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 5, 7, 11 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ando in view of Hashimoto (Us 5856702).

Regarding claim 1, Fig. 1 of Ando shows a resistive structure [7] integrated in a semiconductor substrate [1], comprising:

a trench lined with dielectric material [3] to form a dielectric trench; and

a polysilicon region [4], at least a portion of which is doped, the polysilicon region completely surrounded by the dielectric trench so that the resistive structure is isolated electrically from other components jointly integrated in the semiconductor substrate, and the dielectric region having a width that increases along the resistive structure in which a voltage drop increases (Abstract).

Fig. 1 of Ando shows the most aspect of the instant invention except "wherein portions of the dielectric trench are formed with a plurality of trenches distributed about the polysilicon region to form a single dielectric region." Fig. 6 of Hashimoto shows a resistive structure wherein portions of the dielectric trench [12] are formed with a plurality of trenches [areas

covering the slots 14A-C] distributed about the polysilicon region [16] to form a single dielectric region.

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Hashimoto to the device of Ando in order to have portions of the dielectric trench formed with a plurality of trenches distributed about the polysilicon region to form a single dielectric region to reduce the area dimension of the device.

Regarding claim 5, insofar as understood, Fig. 1 of Ando shows the trench is filled with the doped polysilicon region [4]. Also note that "by implantation" is a process designation, and would thus not carry patentable weight in this claim drawn to a product. See *In re Thorp,* 227 USPQ 964 (Fed. Cir. 1985).

Regarding claim 7, insofar as understood, Fig. 1 of Ando shows said first polysilicon layer is enhanced by angled implantation and has a thickness dimension conforming to the sidewalls of the dielectric region. Also note that "by angle implantation" is a process designation, and would thus not carry patentable weight in this claim drawn to a product. See *In re Thorp,* 227 USPQ 964 (Fed. Cir. 1985).

Regarding claim 11, Fig. 1 of Ando shows the most aspect of the instant invention except "the polysilicon region has a T-shaped cross-sectional configuration with a stem portion filling the at least one trench and a cap portion covering the at least one trench and overlapping a portion of a top surface of the silicon substrate on each side of the at least one trench." Fig. 2 of Hashimoto shows a resistive structure wherein the polysilicon region has a T-shaped cross-sectional configuration with a stem portion filling the at least one trench and a cap portion

covering the at least one trench and overlapping a portion of a top surface of the silicon substrate on each side of the at least one trench.

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Hashimoto to the device of Ando in order to have the polysilicon region having a T-shaped cross-sectional configuration with a stem portion filling the at least one trench and a cap portion covering the at least one trench and overlapping a portion of a top surface of the silicon substrate on each side of the at least one trench to lower resistivity.

Regarding claim 15, Fig. 1 of Ando shows the most aspect of the instant invention except "a plurality of trenches coupled together electrically by metallization." Fig. 5 of Hashimoto shows a plurality of trenches [slots 14A-C] coupled together electrically by metallization [22].

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Hashimoto to the device of Ando in order to have a plurality of trenches coupled together electrically by metallization to have the device operate functionally.

Claims 13-14 and 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ando in view of Tsui et al. (US 6054359), hereinafter Tsui.

Regarding claim 13, Fig. 1 of Ando shows the most aspect of the instant invention except "the polysilicon region comprises first and second layers of polysilicon, the second layer being undoped and the first layer implanted with a dopant." Tsui shows in Fig. 4, a semiconductor device with a resistive structure which has a first-doped polysilicon layer [24] and a second layer of undoped polysilicon [26] (Abstract).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Tsui to the device of Ando in order to have the polysilicon region comprising first and second layers of polysilicon, the second layer being undoped and the first layer implanted with a dopant to improve the contact resistance.

Regarding claim 14, insofar as understood, Fig. 1 of Ando shows the first layer of polysilicon is implanted by angled implantation and has a thickness dimension conforming to the walls of the dielectric-coated at least one trench to prevent complete filling of the at least one trench. Also note that "by implantation" is a process designation, and would thus not carry patentable weight in this claim drawn to a product. See *In re Thorp,* 227 USPQ 964 (Fed. Cir. 1985).

Regarding claim 27, Fig. 1 of Ando shows an integrated resistive structure, comprising:

at least one trench formed in a semiconductor substrate [1];

a dielectric layer [2] entirely coating all walls of the at least one trench; and

a polysilicon region [4] filling the at least one trench.

Fig. 1 of Ando shows the most aspect of the instant invention except "a polysilicon region comprising first and second layers of polysilicon filling the at least one trench, the second layer being undoped and the first layer implanted with a dopant." Tsui shows in Fig. 4, a semiconductor device with a resistive structure which has a first doped polysilicon layer [24] and a second layer of undoped polysilicon [26] (Abstract).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Tsui to the device of Ando in order to have a polysilicon

region comprising first and second layers of polysilicon filling the at least one trench, the second layer being undoped and the first layer implanted with a dopant to improve the contact.

Regarding claim 27, insofar as understood, Fig. 1 of Ando shows the first layer of polysilicon [a doped polysilicon layer] is implanted by angled implantation and has a thickness dimension conforming to the walls of the dielectric-coated at least one trench to fill of the at least one trench. Also note that "by angle implantation" is a process designation, and would thus not carry patentable weight in this claim drawn to a product. See *In re Thorp,* 227 USPQ 964 (Fed. Cir. 1985).

Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ando and Hashimoto as applied to claim 1 above, and further in view of Stone et al. (US 5753391), hereinafter Stone.

Regarding claim 2, the combined teachings of Ando and Hashimoto show the most aspect of the instant invention except "said polysilicon region and said dielectric region have a serpentine pattern, thereby reducing the space requirements of the resistive structure for a given resistance value." Fig. 1 of Stone shows a resistive structure integrated in a semiconductor substrate said polysilicon region [11] and said dielectric region [col. 1, lines 54-56] have a serpentine pattern.

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Stone to the device of Ando and Hashimoto in order to have the polysilicon region and the dielectric region a serpentine-patterned, thereby reducing the space requirements of the resistive structure for a given resistance value to build a compact device.

Regarding claim 3, Fig. 1 of Stone shows said serpentine pattern is formed to include rungs, said rungs are physically connected in parallel together by a metallization [14, 15, 16, 17].

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ando and Hashimoto as applied to claim 1 above, and further in view of Tsui.

Regarding claim 6, the combined teachings of Ando ad Hashimoto show the most aspect of the instant invention except "said polysilicon region comprises two deposited layers of polysilicon, only a first of said layers being enhanced by implantation to lower the values of parasitic capacitances associated with the resistive structure." Tsui shows in Fig. 4, a semiconductor device with a resistive structure which has a first doped polysilicon layer [24] and a second layer of undoped polysilicon [26] (Abstract).

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Tsui to the device of Ando and Hashimoto in order to have said polysilicon region comprised two deposited layers of polysilicon, only a first of said layers being enhanced by implantation to lower the values of parasitic capacitances associated with the resistive structure to improve the contact.

Also note that "by implantation" is a process designation, and would thus not carry patentable weight in this claim drawn to a product. See *In re Thorp*, 227 USPQ 964 (Fed. Cir. 1985).

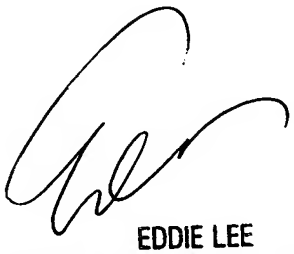
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

jmi



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